RTaW-PEGaSE®

MODULE
Software-Defined X

Validate Your Timing Constraints Before Writing A Single Line Of Code

Key Features

- **Enable the modeling** of real-time software running on processors as tasks communicating via messages and signals, locally or over a communication network,
- **Offer timing-accurate simulation** and worst-case response time analysis for software functions, network transmissions, and sensor-to-actuator timing chains,
- **Provide firm guarantees** that processor loads remain within budget and task timing constraints are met,
- **Enable proper buffer sizing** to prevent message losses,
- **Support Service-Oriented Architectures** (SOME/IP, DDS, MQTT) and ensure services are consistently delivered on time,
- **Support Real-Time Scheduling** for AUTOSAR and POSIX Environments,
- **Support** for modern high-performance computer models with hypervisors,
- **Quantify system extensibility** in terms of spare processor capacity and the number of additional functions and services the architecture can support,
- **Explore architectural and technological design** options on models, enabling performance- and cost-driven design choices early in the design,
- **Leverage Pegase's networking modules** for comprehensive system-level verification for distributed functions.

System-level and Multilayer Modeling

Supports AUTOSAR and Non-AUTOSAR Platforms

DDS, SOME/IP and MQTT Service-Oriented Architectures

Support of CAN (FD, XL), Ethernet, LIN, FlexRay, Wireless, and Heterogeneous Networks

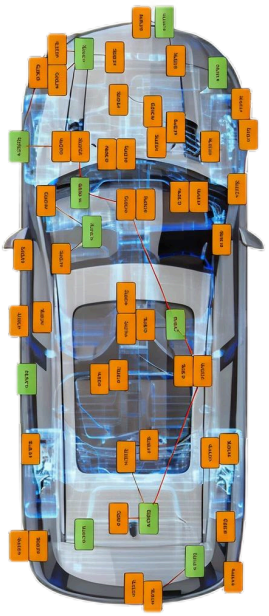
---

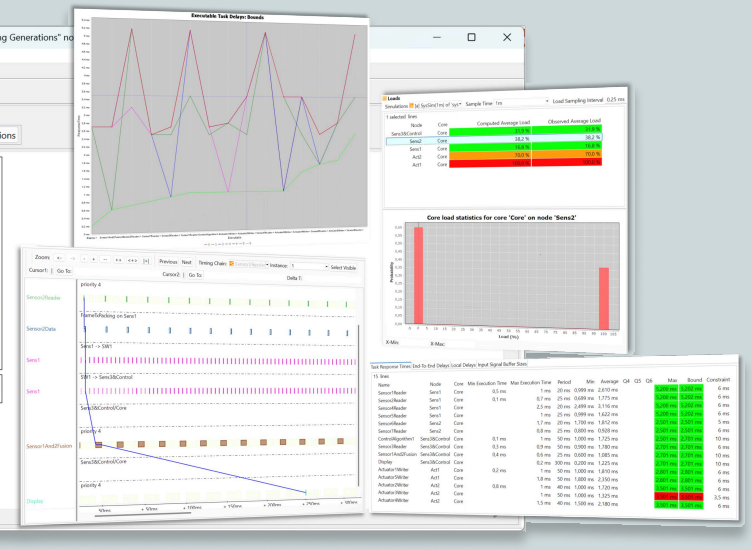
Get in touch with our experts now!

Ask for demo or a free evaluation period

System-Level Modeling

- Enable the modeling of software tasks communicating through messages and signals, locally or over a communication network,
- Support industry standard file formats (e.g. AUTOSAR .arxml) to fit into the overall design flow,
- Allow modeling of system-level timing chains—such as those between sensors and actuators—across processors and networks in the embedded system,
- Support design choices in terms of tasks allocation to hypervisors, cores and processors, scheduling policy and task activation patterns.





Evaluation and Visualization

- Prove correct timing behavior with simulations and worst-case analysis of software functions, network transmissions, and system-level timing chains,
- Ensure optimal performance with guaranteed CPU load compliance,
- Gain insights into complex timing behavior with rich, intuitive visualizations including Gantt charts, load graphs, and histograms.

System-Level Configuration

Seamlessly describe and model all the system timing constraints — from application-level deadlines to communication delays — directly within the architecture model.

Advanced algorithms automatically validate, adjust, and optimize system design choices (e.g. tasks offsets and priorities) to ensure full compliance with all defined timing constraints.

contact@realtimeatwork.com
www.realtimeatwork.com

RTaW-Pegase® module SDV
Version 2025.05